IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants:	Jian Chen et al.		
Title:	Read And Erase Verify Methods And Circuits Suitable For Low Voltage Non-Volatile Memories		
Application No.:	10/552,948	Filing Date:	April 8, 2004
Examiner:	Yoha, Connie C.	Group Art Unit:	2827
Docket No.:	SNDK.284US1	Conf. No.:	6573

Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT

Dear Sir:

Pursuant to 37 C.F.R. §§ 1.56, 1.97 and 1.98, Applicant(s) call(s) the documents listed on the enclosed Form PTO-1449 to the Examiner's attention in this patent application.

Copies of the listed Other Art are enclosed.

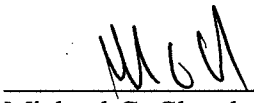
Citation of these documents shall not be construed as (1) an admission that the documents are prior art with respect to the invention or inventions claimed in this application, (2) a representation that a search has been made (other than as indicated by any cited document), or (3) an admission that the cited information is, or is considered to be, material to patentability as defined in § 1.56(b).

This information disclosure statement is submitted under 37 C.F.R. § 1.97(c). The fee of $180.00 has been authorized via EFS to Deposit Account 04-0258. The Commissioner is hereby

authorized to charge any additional fees, which may be required, or credit any overpayment to Deposit Account 04-0258.

FILED VIA EFS

Respectfully submitted,



1-11-08

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